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Security Evaluation and Enhancement of Bistable Ring PUFs

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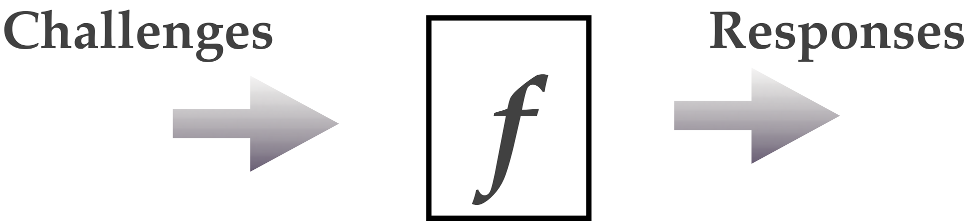
Outline

- Background
  - PUFs
  - Modeling attacks on PUFs
  - Bistable Ring PUF
- Security Evaluation of BR PUFs
  - Modeling the BR PUF
  - Results against BR PUF and variants
- Security Enhancement of BR PUFs
  - XORing BR PUFs to enhance the security
  - Impact on other PUF parameters
- Conclusion and future work

Physical Unclonable Functions

- Map challenges to responses according to physical variations
- Security applications include key storage and authentication



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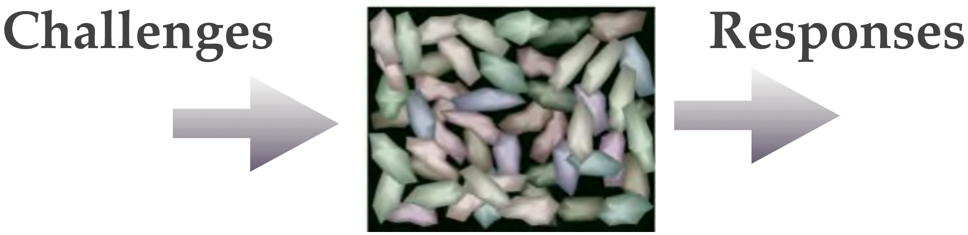


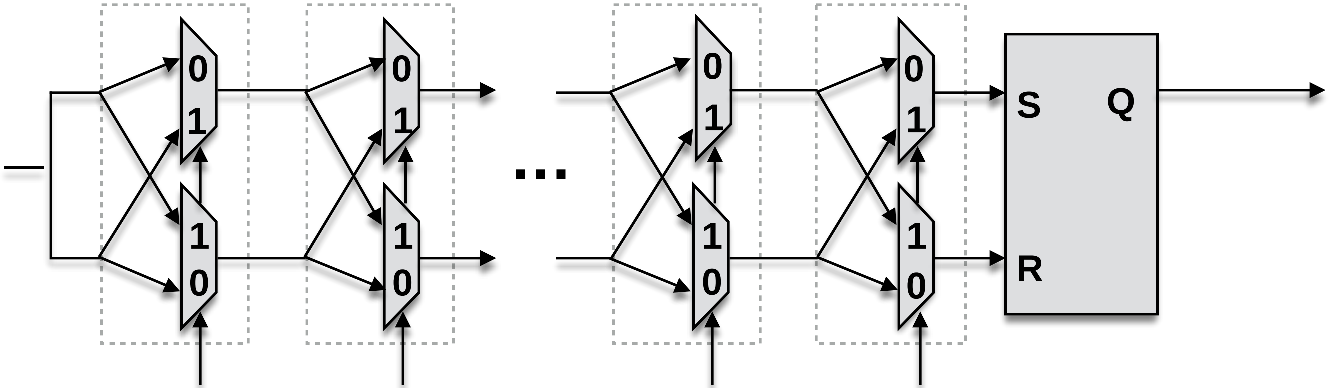
Challenges

Responses

PUF Characterized by Challenge-Response Pairs (CRPs)

- Exponential challenge space
- **Modeling attacks should not be possible**

PUFs and Modeling Attacks



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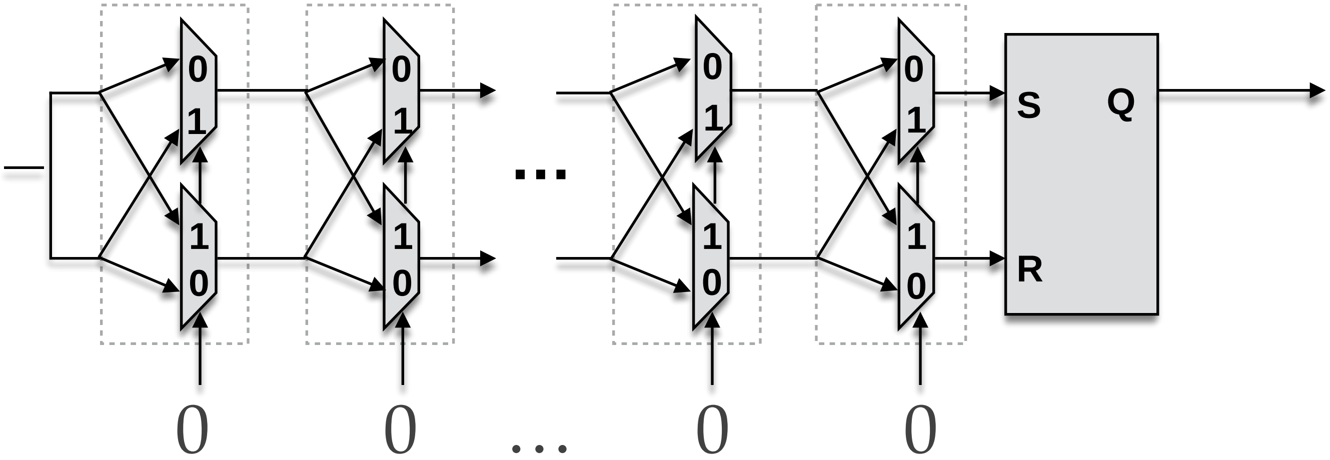

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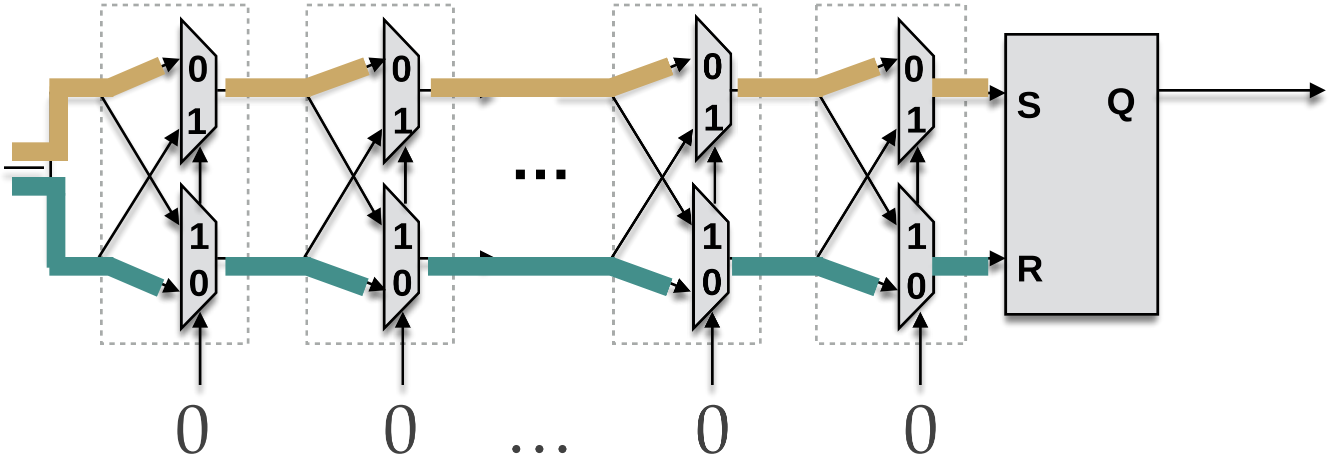

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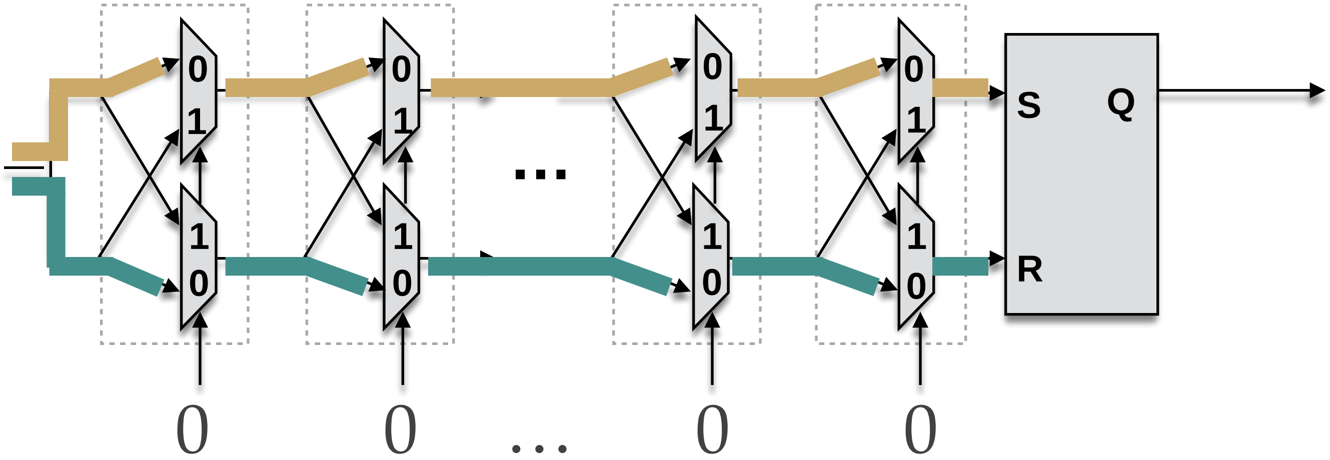

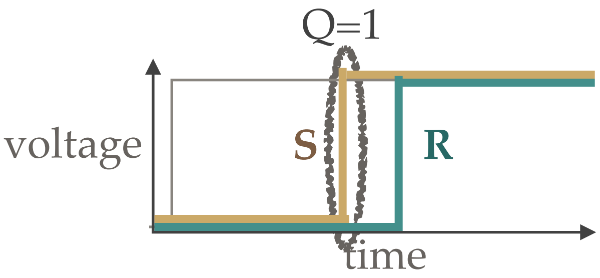

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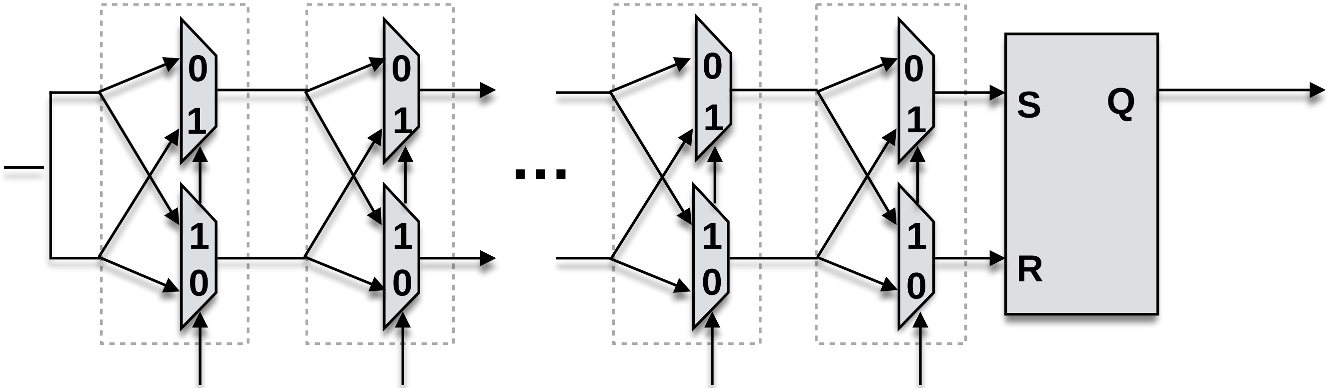

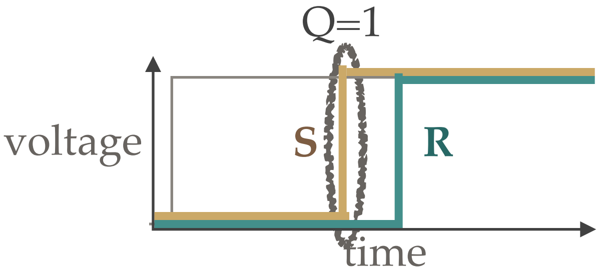

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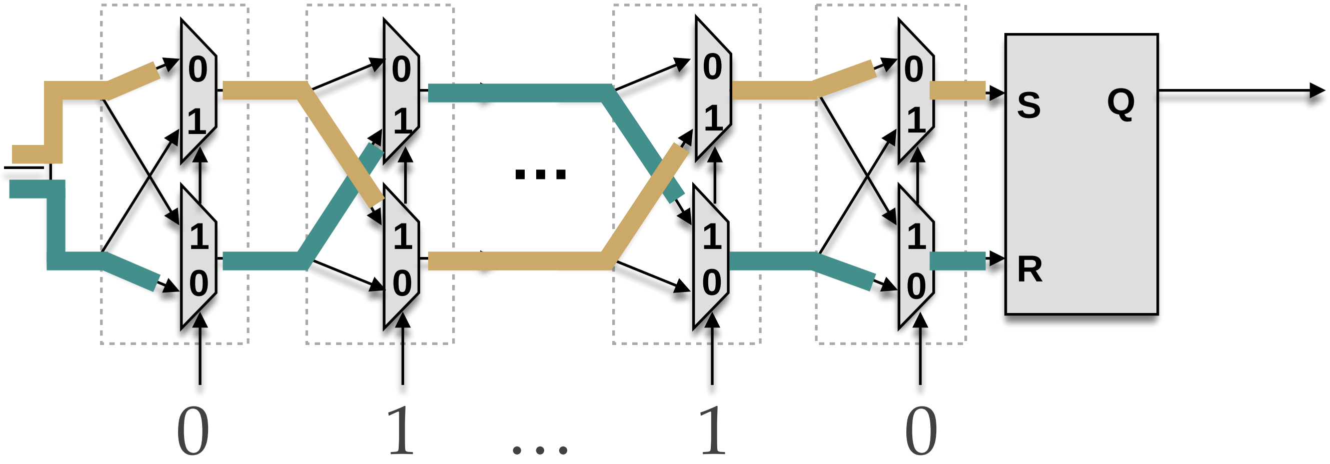

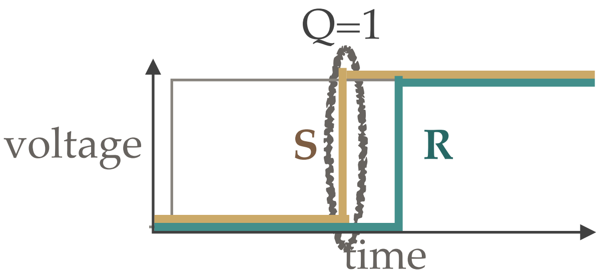

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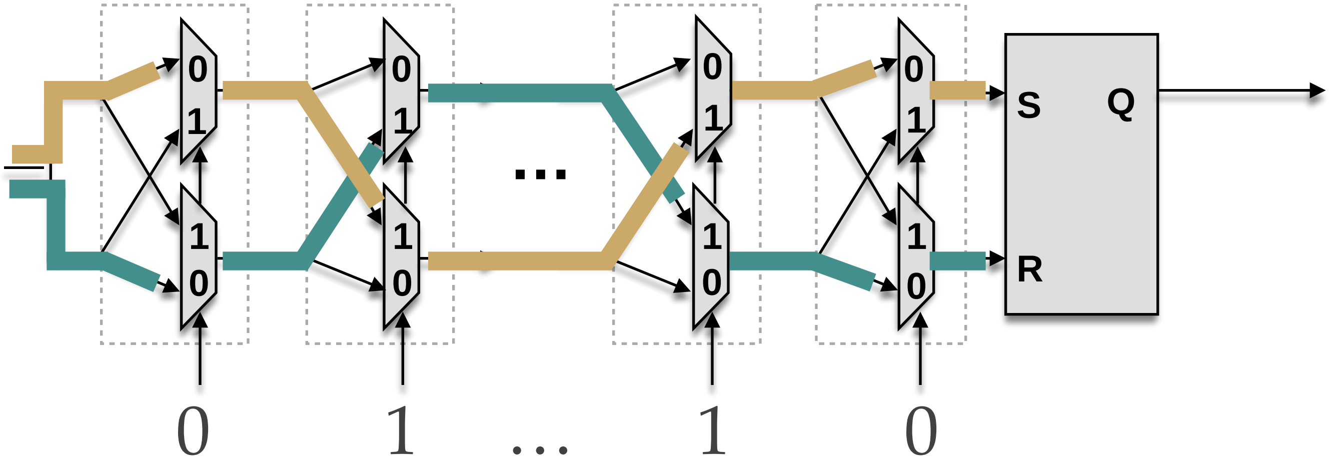

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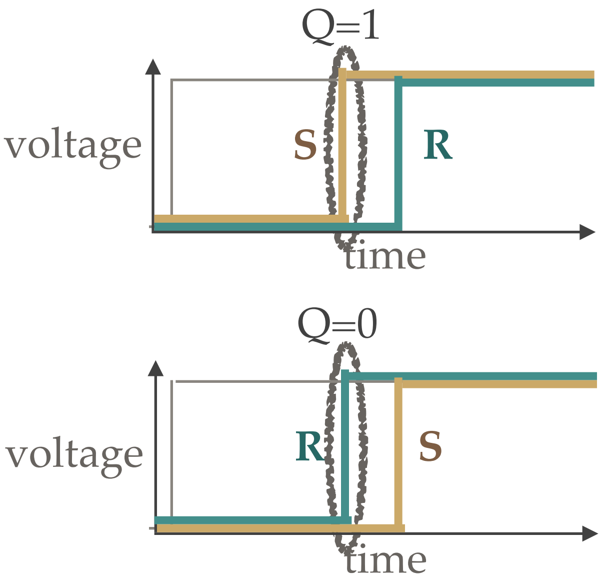

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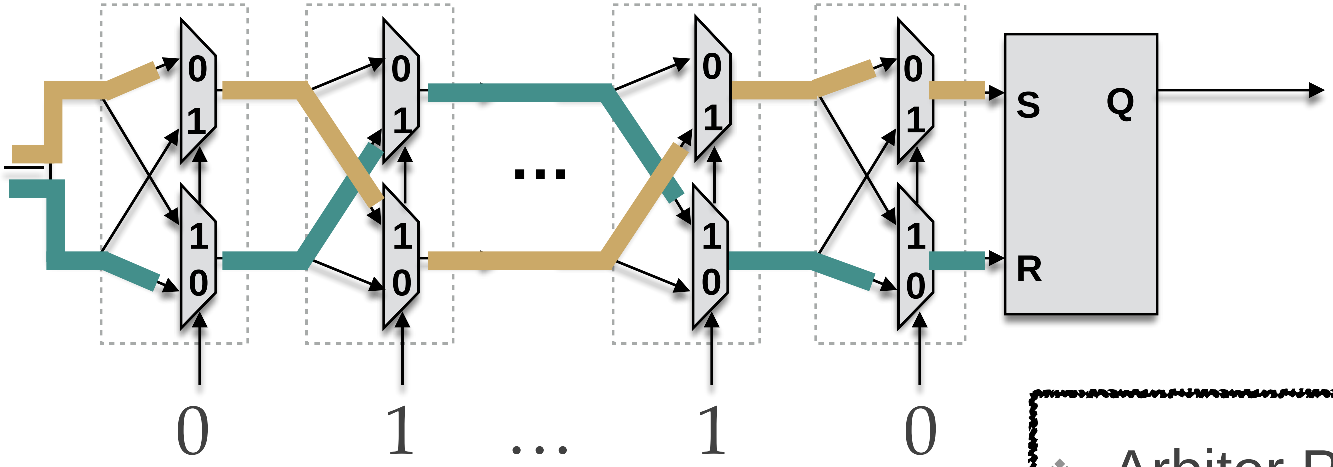

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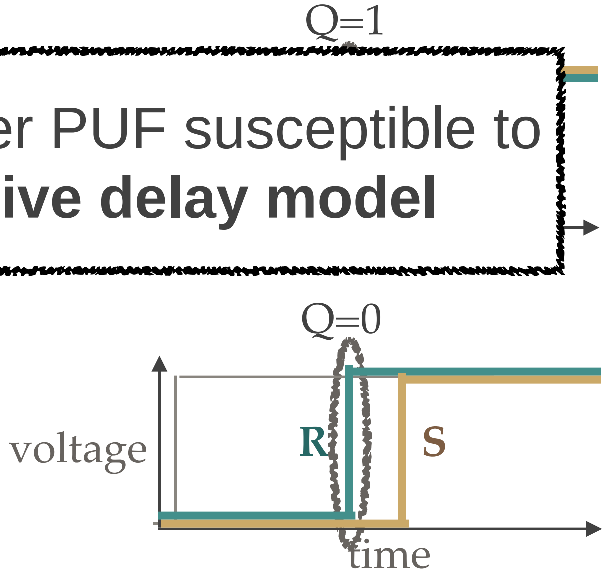
❖ Arbiter PUF susceptible to **additive delay model**



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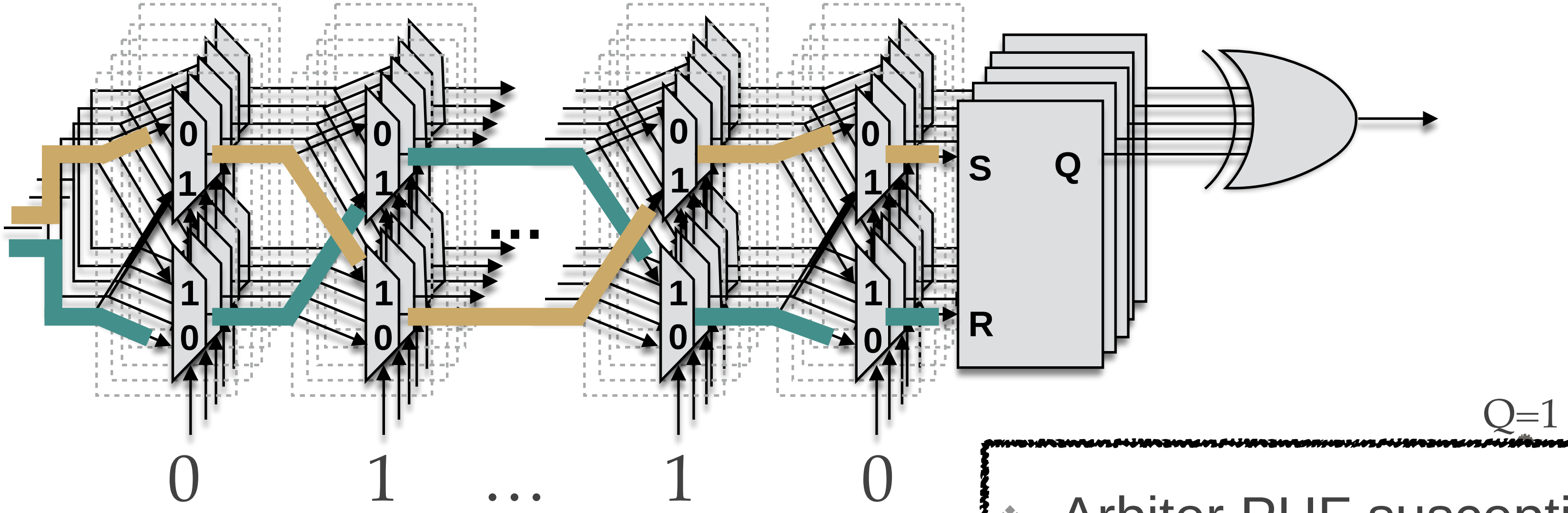

- Challenges: $C_i \in 2^n$ (n= num stages
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- Arbiter PUF susceptible to **additive delay model**

- Arms race of designs versus attacks ongoing….
- XOR PUF[5], Lightweight PUF[3]
- SVM[1], Evolutionary Strategies[6], Logistic Regression[6], ANN[8], Hybrid attacks[4]

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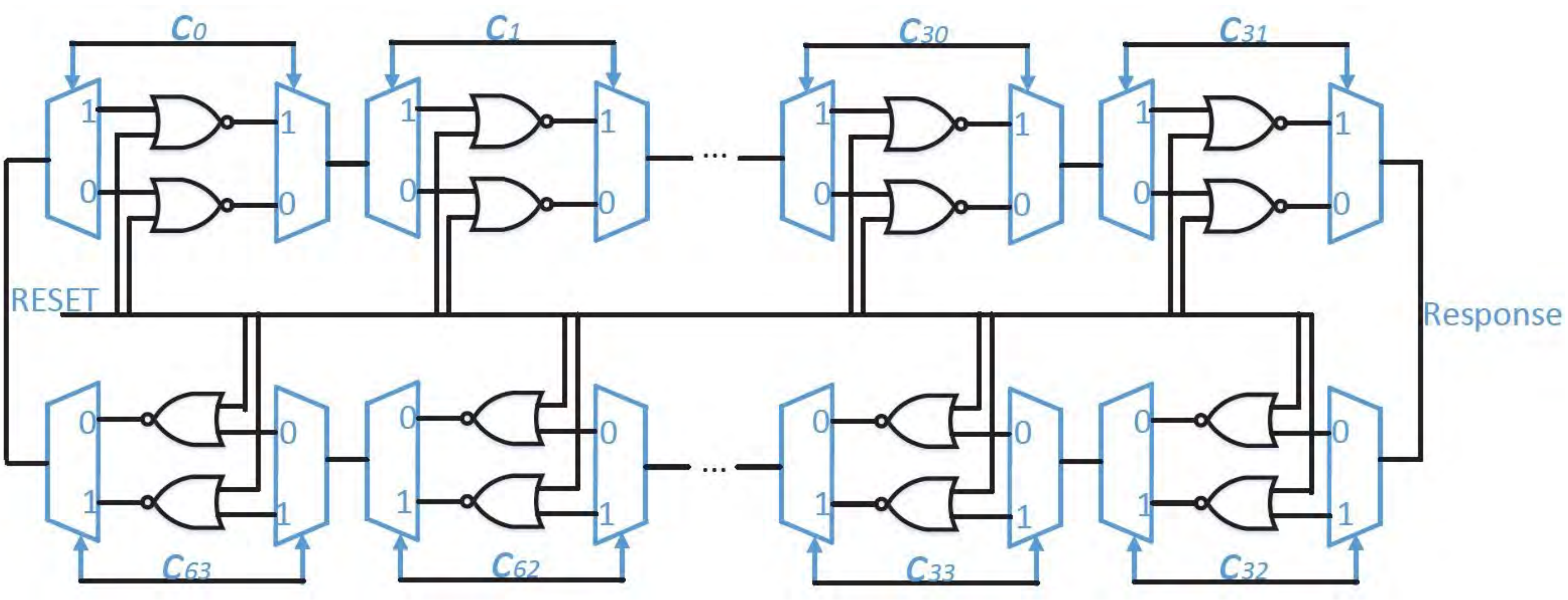
Bistable Ring PUFs

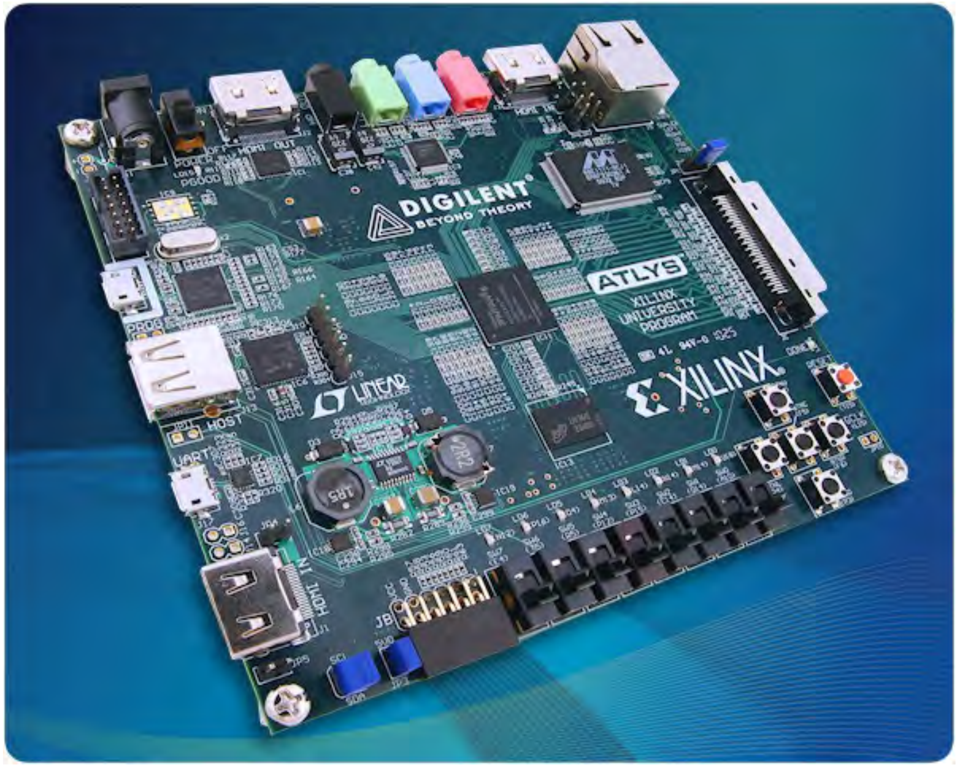
- BR PUF(5) is composed of n-stages, where each stage has two inverting delay elements (NOR gates as an example)
- Each challenge vector configures a unique ring $C_i \in 2^n$ (n= num stages)
- Ring has two stable states $r_i \in \{0,1\}$



(5) Q Chen, et al. *HOST,* 2011

FPGA implementation

BR PUF implemented on Spartan VI FPGA



64-bit BR PUF implementation including peripheral logic, I/O etc

# of slices	3556
# of slice flip flops	***3688***
# of LUTs	***6318***

544 gates to implement only the basic BR PUF

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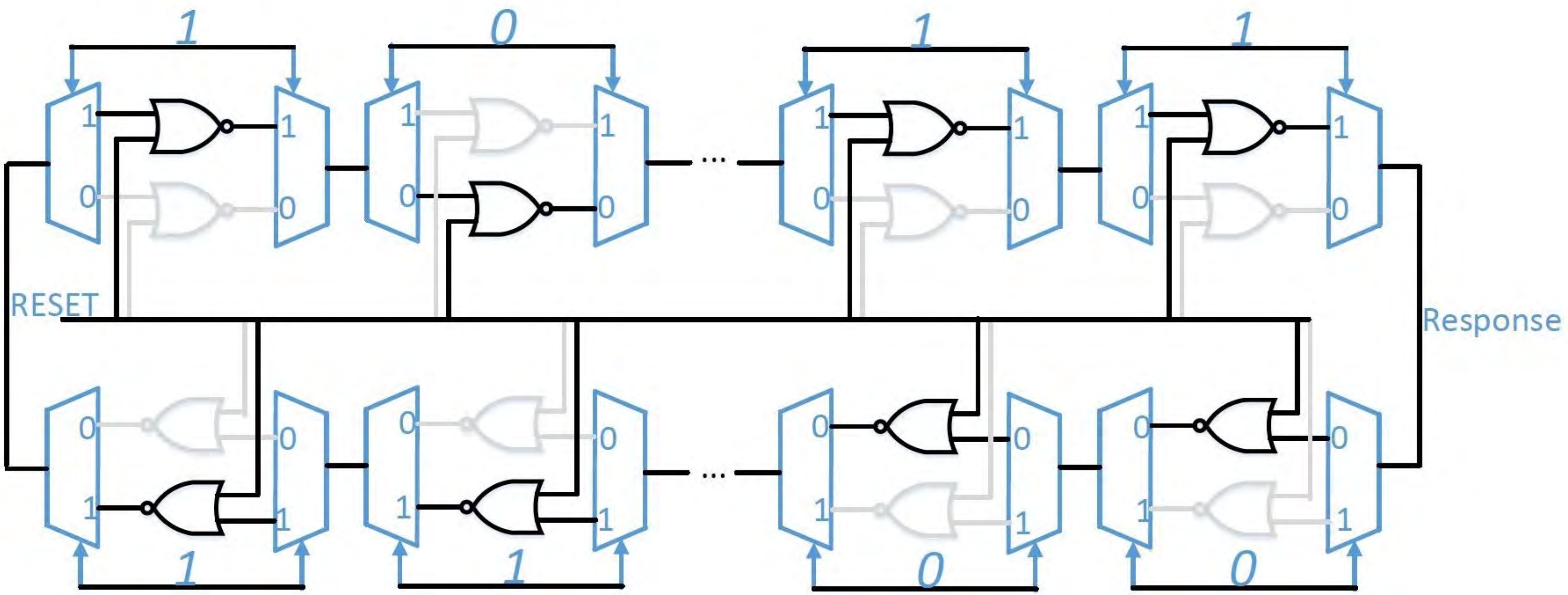
Evaluating Response of BR PUF

1. Apply reset and challenge to configure ring
2. Release reset
3. Read response after allow time for stabilization



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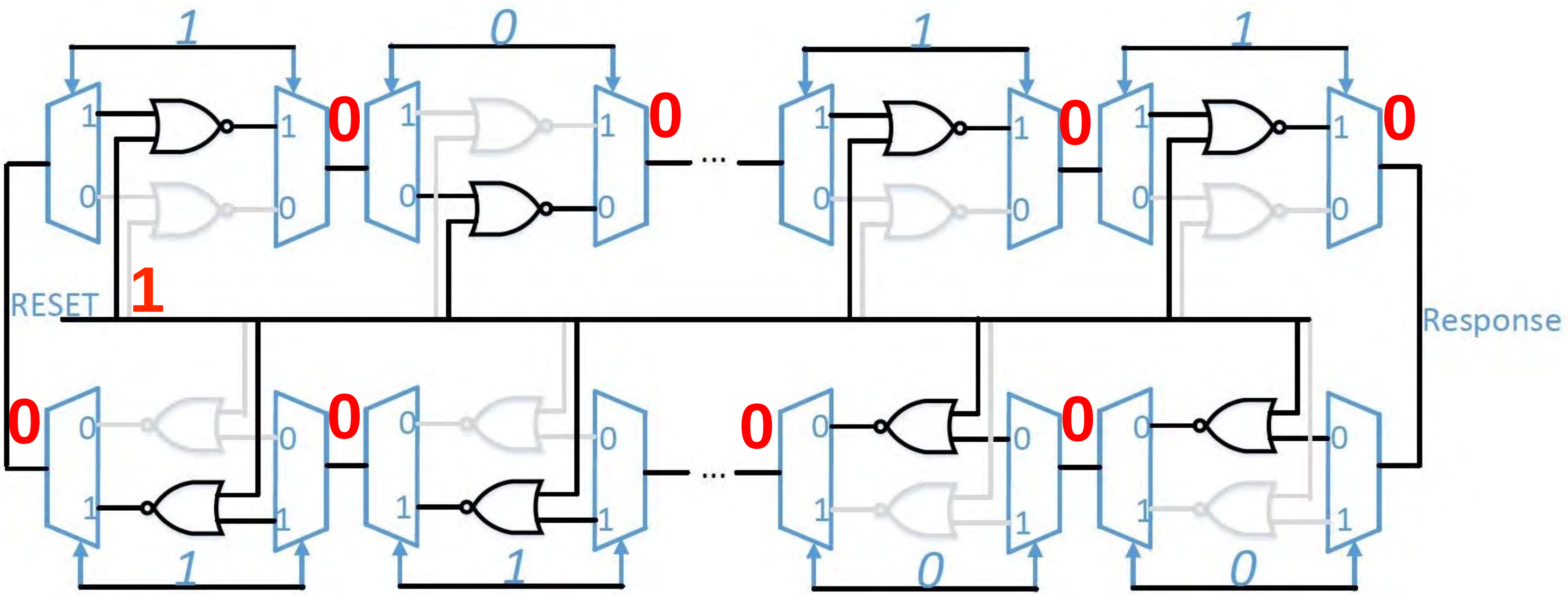

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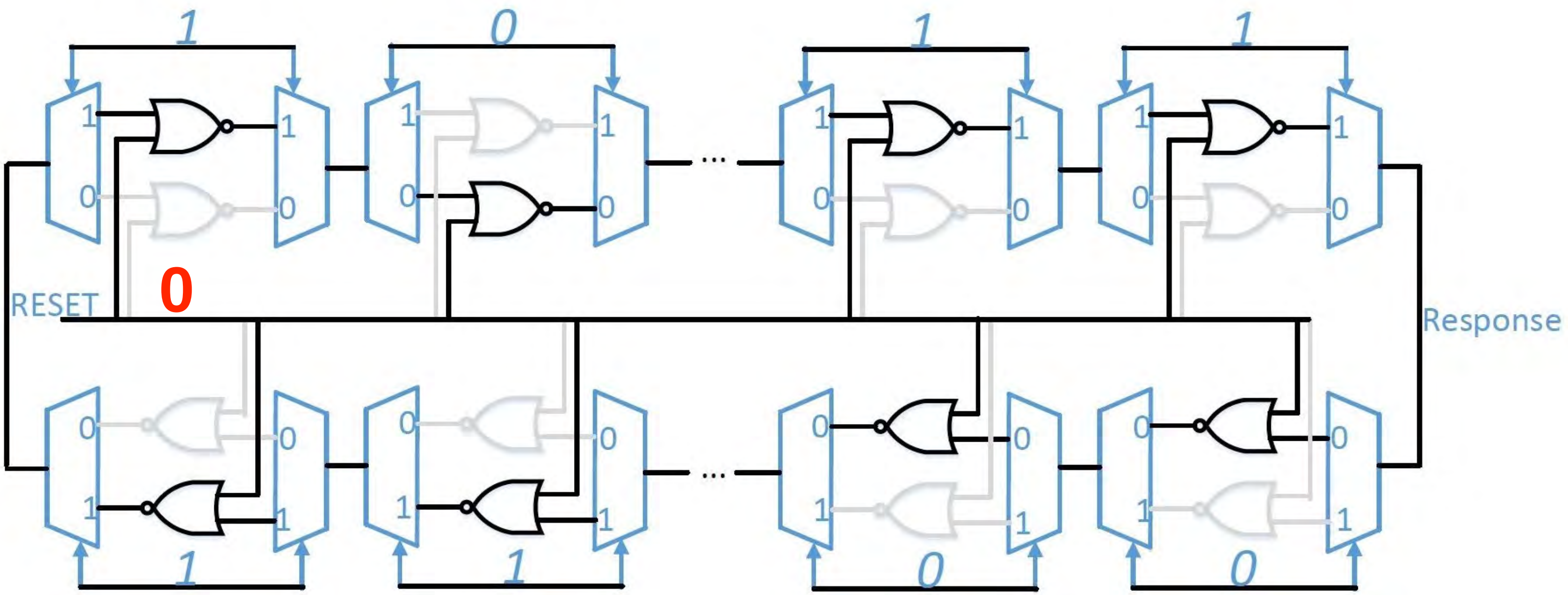

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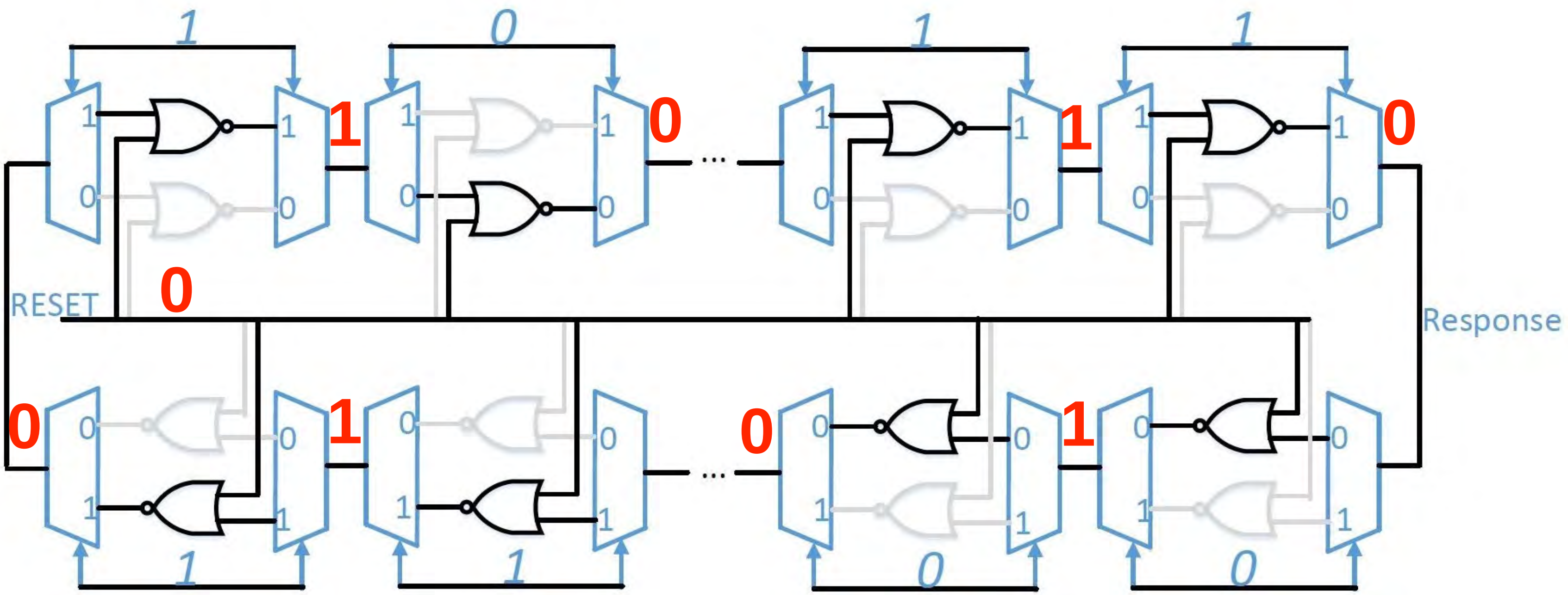

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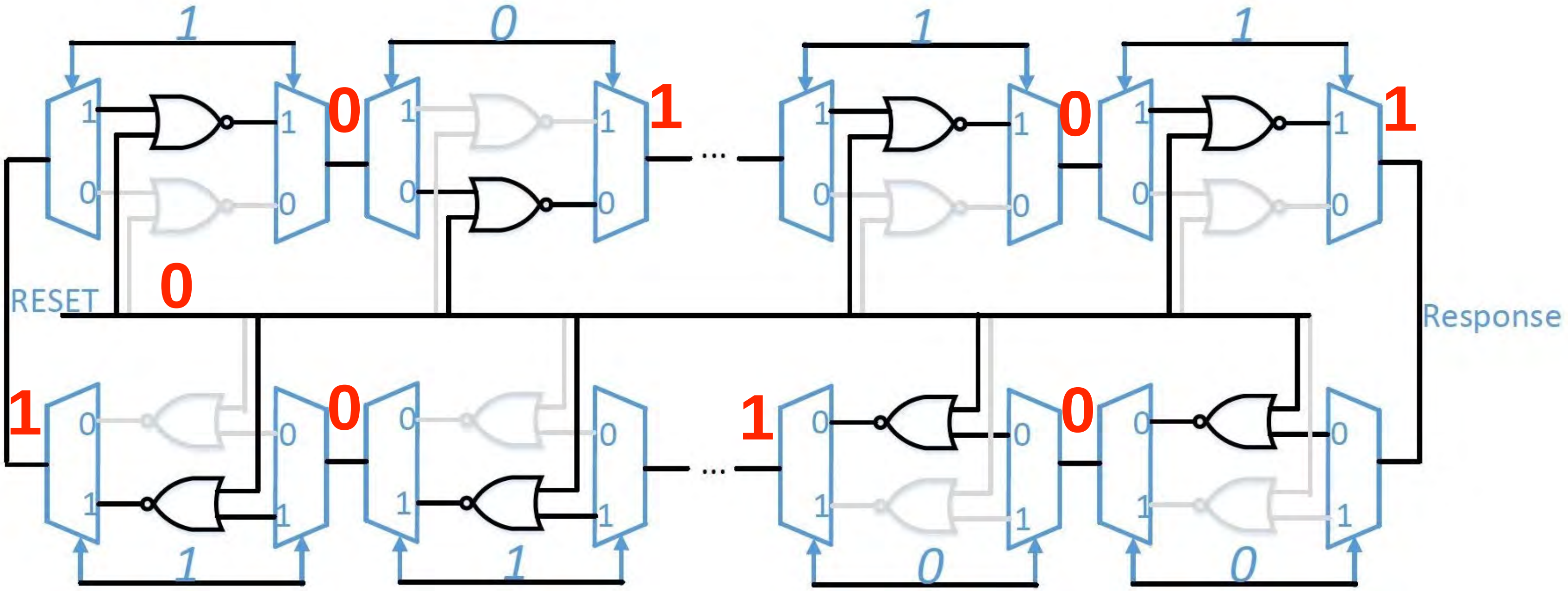
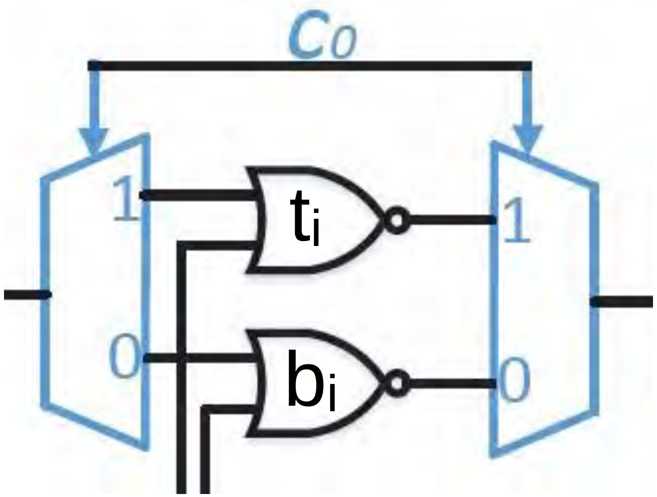


Modeling the BR PUF

- Represent each stage by two weights
- Weights represent tendency to favor a stage output of 1 over stage output of 0
- t_i represents weight of top gate in i^{th} stage
- b_i represents weight of bottom gate in i^{th} stage

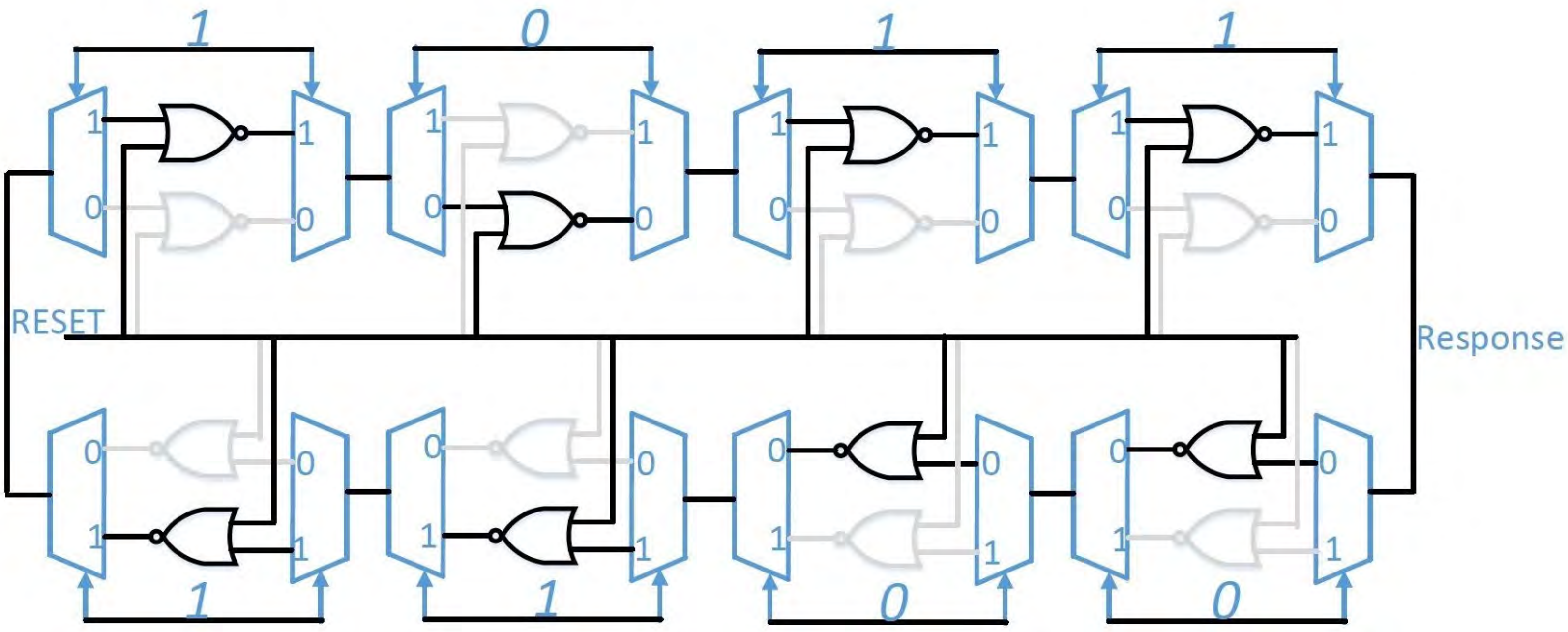


Assumption: there exist weights that explain the challenge response mapping of BR PUF

Example

- Challenge bits select weights, stage index determines signs
- Response tells whether sum is negative or positive
- Additive delay model (like Arbiter PUF)

$$t_0 - b_1 + t_2 - t_3 + b_4 - b_5 + t_6 - t_7$$


1
0
1
1
RESET
Response
1
1
0
0